



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,867	04/12/2001	Shunpei Yamazaki	740756-2294	1394
31780	7590	02/25/2005	EXAMINER	
ERIC ROBINSON				LEWIS, MONICA
PMB 955				
21010 SOUTHBANK ST.				
POTOMAC FALLS, VA 20165				
				ART UNIT
				PAPER NUMBER
				2822

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/832,867	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 November 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14,25-38 and 51-64 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-14,25-28 and 51-64 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 January 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 11/04 and 12/04.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed November 29, 2004.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 11 and 12 disclose that the "coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film." However, this limitation does not appear to be disclosed.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 9-12 and 33-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "the gate

electrode is covered by an insulating film comprising a resin film and at least one of a silicon nitride film and a silicon oxynitride" (For Example: See Claims 9, 10, 33 and 34). In the specification, it appears that the insulating film is not comprised of a resin film and at least one of a silicon nitride film and a silicon oxynitride (For Example: See Page 6 Lines 9-16). Instead, it appears that there are two separate layers.

Finally, it is not clear what is meant by the following: a) "coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film" (For Example: See Claims 11 and 12). The specification discloses a protecting film of silicon nitride or silicon oxynitride and a coloring layer (For Example: See Page 15 and Page 16). It is not clear where the additional layer is disclosed. Claims 11, 12, 35 and 36 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s): a) "coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film" (For Example: See Claims 11 and 12). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1, 2, 5, 6, 13 and 14 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki (U.S. Patent No. 6,501,098).

In regards to claim 1, Yamazaki discloses the following:

a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (101) (For Example: See Figure 1);

b) a channel forming region (104) (For Example: See Figure 1);

c) an n-type impurity region (106a) adjacent to the channel forming region (For Example: See Figure 1);

d) an n-type impurity region (106b) adjacent to the n-type impurity region (For Example: See Figure 1);

Art Unit: 2822

- e) an n-type impurity region (108) adjacent to the n-type impurity region (For Example: See Figure 1);
- f) a gate insulating layer (103) provided over the active layer (For Example: See Figure 1);
- g) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);
- h) a first conductive film (113) provided over the gate insulating layer (For Example: See Figure 1); and
- i) a second conductive film (114) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claim 2, Yamazaki discloses the following:

- a) a driver circuit having a n-channel TFT over a substrate (For Example: See Column 27 Lines 23-57);
- b) pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1 and Figure 29);
- c) a channel forming region (For Example: See Figure 1);
- d) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1);
- e) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- f) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- g) a gate insulating layer provided over the active layer (For Example: See Figure 1);
- h) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);
- i) a first conductive film provided over the gate insulating layer (For Example: See Figure 1); and

Art Unit: 2822

j) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claims 5 and 6, Yamazaki discloses the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum (For Example: Column 7 Lines 44-58).

In regards to claims 13 and 14, Yamazaki discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 30 Lines 46-58).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of *Silicon Processing for the VLSI Era* by S. Wolf.

In regards to claims 3 and 4, Yamazaki discloses the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride (For Example: See Column 7 Lines 48-58).

In regards to claims 3 and 4, Yamazaki fails to disclose the following:

a) the second conductive film comprises tungsten.

However, Wolf discloses the use of tungsten as a gate material (For Example: See Pages 398 and 399). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include the use of tungsten as disclosed in Wolf because it aids in providing low resistivities (For Example: See Page 398).

Additionally, since Yamazaki and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Yamazaki.

12. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098).

In regards to claims 7 and 8, Yamazaki fails to disclose the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, the n-type impurity region includes an n-type impurity element in concentrations of from 2×10^{16} to 5×10^{19} atoms/cm³, and the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{16} to 5×10^{19} atoms/cm³.

However, the applicant has not established the critical nature of concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, 2×10^{16} to 5×10^{19} atoms/cm³, and 1×10^{16} to 5×10^{19} atoms/cm³. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Art Unit: 2822

13. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Yamazaki (U.S. Patent No. 6,093,934).

In regards to claims 9 and 10, Yamazaki fails to disclose the following:

a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Yamazaki discloses a gate electrode (307) covered by an insulating film (316) comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (For Example: See Column 9 Lines 65-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Yamazaki because it aids in keeping the device from shortening out (For Example: See Figure 3c).

Additionally, since Yamazaki and Yamazaki are both from the same field of endeavor, the purpose disclosed by Yamazaki would have been recognized in the pertinent art of Yamazaki.

14. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Yamazaki (U.S. Patent No. 6,093,934) and Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claims 11 and 12, Yamazaki fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film.

However, Shohara discloses a coloring layer (217) provided between the resin film (13) and the silicon nitride film (216) or between the resin film and the silicon oxynitride film (For Example: See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill

in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

15. Claims 25, 26, 29-32 and 35-38 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claim 25, Yamazaki discloses the following:

- a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1);
- b) a channel forming region (For Example: See Figure 1);
- c) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- e) an n-type impurity region (adjacent to the n-type impurity region (For Example: See Figure 1);
- f) a gate insulating layer provided over the active layer (For Example: See Figure 1);
- g) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);
- h) a first conductive film provided over the gate insulating layer (For Example: See Figure 1); and

i) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claim 25, Yamazaki fails to disclose the following:

- a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer (217) provided over the gate electrode (16) (For Example: See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claim 26, Yamazaki discloses the following:

- a) a driver circuit having a n-channel TFT over a substrate (For Example: See Column 27 Lines 23-57);
- b) pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1 and Figure 29);
- c) a channel forming region (For Example: See Figure 1);
- d) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1);
- e) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- f) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);

Art Unit: 2822

g) a gate insulating layer provided over the active layer (For Example: See Figure 1);

h) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);

i) a first conductive film provided over the gate insulating layer (For Example: See Figure 1); and

j) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claim 26, Yamazaki fails to disclose the following:

a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer provided over the gate electrode (For Example: See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 29 and 30, Yamazaki discloses the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum (For Example: Column 7 Lines 44-58).

In regards to claims 31 and 32, Yamazaki fails to disclose the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, the n-type impurity region includes an n-type impurity element in concentrations of from 2×10^{16} to 5×10^{19} atoms/cm³, and the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{16} to 5×10^{19} atoms/cm³.

Art Unit: 2822

However, the applicant has not established the critical nature of concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, 2×10^{16} to 5×10^{19} atoms/cm³, and 1×10^{16} to 5×10^{19} atoms/cm³. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

In regards to claims 35 and 36, Yamazaki fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film.

However, Shohara discloses a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film (For Example: See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 37 and 38, Yamazaki discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 30 Lines 46-58).

Art Unit: 2822

16. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Shohara et al. (U.S. Patent No. 6,238,754) and *Silicon Processing for the VLSI Era* by S. Wolf.

In regards to claims 27 and 28, Yamazaki discloses the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride (For Example: See Column 7 Lines 48-58).

In regards to claims 27 and 28, Yamazaki fails to disclose the following:

a) the second conductive film comprises tungsten.

However, Wolf discloses the use of tungsten as a gate material (For Example: See Pages 398 and 399). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include the use of tungsten as disclosed in Wolf because it aids in providing low resistivities (For Example: See Page 398).

Additionally, since Yamazaki and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Yamazaki.

17. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Shohara et al. (U.S. Patent No. 6,238,754) and Yamazaki (U.S. Patent No. 6,093,934).

In regards to claims 33 and 34, Yamazaki fails to disclose the following:

a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Yamazaki discloses a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (For Example: See

Art Unit: 2822

Column 9 Lines 65-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Yamazaki because it aids in keeping the device from shortening out (For Example: See Figure 3c).

Additionally, since Yamazaki and Yamazaki are both from the same field of endeavor, the purpose disclosed by Yamazaki would have been recognized in the pertinent art of Yamazaki.

18. Claims 51, 52, 55-58, 63 and 64 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Takemura et al. (U.S. Patent No. 6,835,607).

In regards to claim 51, Yamazaki discloses the following:

- a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1);
- b) a channel forming region (For Example: See Figure 1);
- c) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- e) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);
- f) a gate insulating layer provided over the active layer (For Example: See Figure 1);
- g) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);
- h) a first conductive film provided over the gate insulating layer (For Example: See Figure 1); and

Art Unit: 2822

i) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claim 51, Yamazaki fails to disclose the following:

a) the gate insulating layer has a greater thickness over the channel forming region than over the n-type impurity region.

However, Takemura et al. ("Takemura") discloses a gate insulating layer (6) that has a greater thickness over the channel forming region (3) than over the impurity region (2) (For Example: See Figure 2d). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate insulating layer that has a greater thickness over the channel forming region than over the impurity region as disclosed in Takemura because it aids in protecting the reliability of the film (For Example: See Column 4 Lines 3-6).

Additionally, since Yamazaki and Takemura are both from the same field of endeavor, the purpose disclosed by Takemura would have been recognized in the pertinent art of Yamazaki.

In regards to claim 52, Yamazaki discloses the following:

a) a driver circuit having a n-channel TFT over a substrate (For Example: See Column 27 Lines 23-57);

b) pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1 and Figure 29);

c) a channel forming region (For Example: See Figure 1);

d) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1);

e) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1);

f) an n-type impurity region adjacent to the n-type impurity region
(For Example: See Figure 1);

g) a gate insulating layer provided over the active layer (For Example: See Figure 1);

h) a gate electrode provided over the gate insulating layer (For Example: See Figure 1);

i) a first conductive film provided over the gate insulating layer (For Example: See Figure 1); and

j) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1).

In regards to claim 52, Yamazaki fails to disclose the following:

a) the gate insulating layer has a greater thickness over the channel forming region than over the n-type impurity region.

However, Takemura discloses a gate insulating layer that has a greater thickness over the channel forming region than over the impurity region (For Example: See Figure 2d). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate insulating layer that has a greater thickness over the channel forming region than over the impurity region as disclosed in Takemura because it aids in protecting the reliability of the film (For Example: See Column 4 Lines 3-6).

Additionally, since Yamazaki and Takemura are both from the same field of endeavor, the purpose disclosed by Takemura would have been recognized in the pertinent art of Yamazaki.

Art Unit: 2822

In regards to claims 55 and 56, Yamazaki discloses the following:

a) the first conductive film comprises tungsten, and the second gate electrode comprises aluminum (For Example: Column 7 Lines 44-58).

In regards to claims 57 and 58, Yamazaki fails to disclose the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, the n-type impurity region includes an n-type impurity element in concentrations of from 2×10^{16} to 5×10^{19} atoms/cm³, and the n-type impurity region includes an n-type impurity element in concentrations from 1×10^{16} to 5×10^{19} atoms/cm³.

However, the applicant has not established the critical nature of concentrations from 1×10^{20} to 1×10^{21} atoms/cm³, 2×10^{16} to 5×10^{19} atoms/cm³, and 1×10^{16} to 5×10^{19} atoms/cm³. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

In regards to claims 63 and 64, Yamazaki discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 30 Lines 46-58).

19. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Takemura et al. (U.S. Patent No. 6,835,607) and *Silicon Processing for the VLSI Era* by S. Wolf.

In regards to claims 53 and 54, Yamazaki discloses the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride (For Example: See Column 7 Lines 48-58).

In regards to claims 53 and 54, Yamazaki fails to disclose the following:

- a) the second conductive film comprises tungsten.

However, Wolf discloses the use of tungsten as a gate material (For Example: See Pages 398 and 399). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include the use of tungsten as disclosed in Wolf because it aids in providing low resistivities (For Example: See Page 398).

Additionally, since Yamazaki and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Yamazaki.

20. Claims 59 and 60 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Takemura et al. (U.S. Patent No. 6,835,607) and Yamazaki (U.S. Patent No. 6,093,934).

In regards to claims 59 and 60, Yamazaki fails to disclose the following:

- a) the gate electrode is covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride films.

However, Yamazaki discloses a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film (For Example: See Column 9 Lines 65-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate electrode covered by an insulating film comprising a resin film and one of a silicon nitride film and a silicon oxynitride film as disclosed in Yamazaki because it aids in keeping the device from shortening out (For Example: See Figure 3c).

Art Unit: 2822

Additionally, since Yamazaki and Yamazaki are both from the same field of endeavor, the purpose disclosed by Yamazaki would have been recognized in the pertinent art of Yamazaki.

21. Claims 61 and 62 are rejected under 35 U.S.C. 103(a) as obvious over Yamazaki (U.S. Patent No. 6,501,098) in view of Takemura et al. (U.S. Patent No. 6,835,607), Yamazaki (U.S. Patent No. 6,093,934) and Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claims 61 and 62, Yamazaki fails to disclose the following:

a) a coloring layer is provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film.

However, Shohara discloses a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film (For Example: See Column 13 Lines 7-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided between the resin film and the silicon nitride film or between the resin film and the silicon oxynitride film as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

Art Unit: 2822

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
February 17, 2005



*Mary Wilczewski
Primary Examiner*